REMARKS

I. Introduction

In response to the Office Action dated March 3, 2006, Applicant has incorporated the subject matter of claim 2 into claim 1, subject matter of claim 9 into claim 8, and subject matter of claim 13 into claim 12. Claims 2, 9 and 13 are canceled, without prejudice or disclaimer. The dependency of claims 3-4, 10 and 14 have been amended. No new matter has been added.

For the reasons set forth below, Applicant respectfully submits that all pending claims are patentable over the cited prior art references.

II. The Rejection Of Claims 1-2, 4-5, 7-9 and 11-13 Under 35 U.S.C. § 103

Claims 1-2, 4-5, 7-9 and 11-13 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicants' Admitted Prior Art (AAPA) in view of USP No. 6,985,483 to Mehrotra. Claims 2, 9 and 13 are canceled, rendering the rejection thereto moot. For the remaining claims, Applicant respectfully requests traverses this rejection for at least the following reasons.

Claim 1

Claim 1 recites in-part conducting a search of a SRAM and DRAM lookup table including searching an SRAM portion for routing information.

A. The First Memory Device Of Mehrotra Does Not Store Routing Information

Mehrotra describes a method for determining an output port corresponding to a next node/hop to which a packet is to be directed in a computer network. Specifically, Mehrotra teaches constructing a network address lookup data structure based on variable-length network address prefixes (col. 5, lines 33-36). The data structure is stored in a first (on-chip SRAM) memory device, while a set of output port identifiers corresponding to the network address prefixes is stored in a second (off-chip DRAM) memory device. The data structure is traversed based on bits in an input address to determine a location corresponding to the longest network

address prefix that matches the input address (col. 12, lines 27-40). The determined location in the data structure is then used to determine an offset in the second memory device for the output port identifier corresponding to the input address (col. 10, line 54 to col. 11, line 30 and lines 54-60).

However, Applicant respectfully submits that the first on-chip SRAM memory device of Mehrotra does not store any next hop address information. Indeed, Mehrotra expressly states that "according to an important aspect of the invention, these next hop addresses are omitted from the actual data structure stored in memory of a processor that performs the address lookups (col. 8, lines 11-20)." Rather, the next hop addresses are stored in an off-chip DRAM memory device (col. 8, lines 38-49).

Accordingly, for at least these reasons, Applicant submits that Mehrotra does not disclose an on-chip SRAM memory device for storing any address information, let alone disclose searching this SRAM memory device for routing information. Thus, as each and every limitation must be either disclosed or suggested by the cited prior art in order to establish a *prima facie* case of obviousness (see, **M.P.E.P. § 2143.03**), and Mehrotra fails to do so, Applicant respectfully submits that claim 1 is patentable over the cited prior art.

B. Mischaracterization of Mehrotra

In rejecting the foregoing claimed subject matter, the Examiner directs the Applicant to col. 14 of Mehrotra and to note "the teachings of SRAM and DRAM [of Mehrotra] and the obviousness of searching the lowest cost memory first before resorting to a search of the higher "cost" memory (see, page 2, last paragraph to page 3, 1st paragraph of Office Action)." Applicant respectfully disagrees.

However, Applicant respectfully submits that the Examiner has mischaracterized Mehrotra. Specifically, at the cited section, Mehrotra discloses that conventional memory accesses require 8 DRAM accesses, each of which has an access cost of 60 ns per random read/write (col. 15, lines 1-6). To cure this problem, Mehrotra suggests using extra off-chip DRAM memory to reduce DRAM accesses (col. 15, lines 19-22), rather than resorting to a

search of "the lowest cost memory" before the "higher cost memory" as interpreted by the pending rejection.

Furthermore, Applicant respectfully submits that the statement "the obviousness of searching the lowest "cost" memory first before resorting to a search of the higher "cost" memory" as a prelude to the rejection is not a proper basis for rejecting Applicant's claims, as this statement is directed to an ***opinion*** rather than what is taught by the prior art. Applicant respectfully submits that an opinion cannot be relied on to replace the deficiency of a prior art reference. If the pending rejection intended to take Official Notice that the differences between Mehrotra and the present invention as recited in the rejected claims are well-known in the art, then pursuant to **M.P.E.P. § 2144.03**, Applicant respectfully traverses such an assertion and request the next Office Action to cite one or more references in support of this position (see, second paragraph, last three lines of **M.P.E.P. § 2144.03**, which requires the Examiner to cite a reference in support of his allegation of Official Notice when Applicant traverses).

C. Mehrotra Does Not Teach Subsequent Process If Routing Information Is Found Or Not Found

Claim 1, which incorporates the subject matter of now-canceled claim 2, recites in-part a router including a router table implemented as a DRAM and SRAM lookup table, and a switch control unit for searching an SRAM portion, wherein if routing information is found in the SRAM portion, no search is performed in the DRAM portion, and wherein if no routing information is found in the SRAM portion, searching a DRAM portion of said SRAM and DRAM lookup table.

Applicant respectfully submits that Mehrotra does not disclose the foregoing claimed features. In fact, any disagreement would expressly depart from the disclosure of Mehrotra, because Mehrotra specifically requires multiple DRAMS to be operated in parallel to achieve a high throughput (col. 14, lines 63-65). Particularly, Mehrotra discloses that next hop addresses are stored in the DRAM off-chip memory (e.g., each of the rows 138-154 in the DRAM off-chip memory stores a set of next hop addresses, col. 8, lines 48-67). Thus, the DRAM off-chip

memory needs to be accessed prior to forwarding a data packet so as to retrieve a next hop address. Accordingly, the action of accessing the DRAM memory is required, and is not optional. Thus, Mehrotra fails to arrive at the claimed invention, because Mehrotra does not disclose that if routing information is found in the SRAM portion, no search is performed in the DRAM portion.

D. No Motivation To Combine the AAPA and Mehrotra

To establish a *prima facie* case of obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings. The teaching or suggestion to make the claimed combination must be found in the prior art. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Applicant respectfully asserts that the Examiner has not provided a sufficient motivation to combine the references. The Examiner provided the following description with respect to the combination:

> "It would have been obvious to one o ordinary skill in the art at the time of the invention to have solved the problem existing in the prior art comprising latency in DRAM based router memories as stated in the AAPA, in light of the teachings of Mehrotra et al, in order to provide a method of routing data at speeds which make the said routers efficient and economical to use."

However, Applicant respectfully submits that the foregoing "motivation" is insufficient. Specifically, the Examiner has not suggested a motivation to combine the AAPA and Mehrotra, and instead has merely provided two facts known in the art that do not support a conclusion of motivation. In fact, the AAPA does not appear to be concerned with how packets should be routed. Rather, the AAPA raises the question of time consumption associated with searching a routing table in which destination addresses are randomly stored.

Furthermore, that one can modify a data routing method to make a router more efficient is not in itself a particular motivation to modify the router taught by the AAPA. Instead, it appears the Examiner has impermissibly used hindsight in an attempt to reconstruct Applicant's

invention. It is improper to use Applicant's disclosure as the motivation to combine the particular teachings in the cited references: "The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in Applicant's disclosure, " M.P.E.P 2143, citing *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991).

Indeed, it appears the pending rejection has impermissibly used hindsight in an attempt to reconstruct Applicant's invention by utilizing Applicant's specification inadvertently as a guide to pick and choose the selected elements from various references so as to reach the claimed invention. Hindsight reconstruction, using applicant's claims as a template to reconstruct the invention by **picking and choosing** isolated disclosures from the prior art, is impermissible. For example, in *In re Fritch*, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1784 (Fed. Cir. 1992), the Federal Circuit stated:

> It is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious. This court has previously stated that one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention. (citations and quotations omitted)

Applicant respectfully submits that the pending rejection has not provided any motivation to modify the AAPA other than to rely on the level of skill in the art, which is impermissible. *See Al-Site Corp. v. VSI Int'l Inc.*, 174 F.3d 1308, 50 USPQ2d 1161 (Fed. Cir. 1999).

In this regard, Applicant would, again, stress that **the mere identification of claim features in disparate references does not establish the requisite realistic motivation** to support the ultimate legal conclusion of obviousness under 35 U.S.C. §103. *Grain Processing Corp. v. American-Maize Products Co.*, 840 F.2d 902, 5 USPQ2d 1788 (Fed. Cir. 1988).

For all of the foregoing reasons, the proposed combination fails to establish *prima facie* obviousness of the pending claims.

Claim 5

Claim 5 recites in-part using routing identification information for accessing an SRAM portion of a routing table for routing information and, if no entry corresponding to the routing

identification information is found in the SRAM portion, accessing a DRAM portion of said routing table.

However, Mehrotra does not determine whether an entry corresponding to a next hop address is found in the SRAM on-chip memory, let alone access the DRAM off-chip memory if such entry is not found.

Also, as discussed with respect to the two-stage process above, the DRAM off-chip memory stores next hop addresses, which requires the DRAM off-chip memory to be accessed. This reinforces the fact that Mehrotra does not teach the determination of such entry.

Thus, as each and every limitation must be either disclosed or suggested by the cited prior art in order to establish a *prima facie* case of obviousness (see, **M.P.E.P. § 2143.03**), and the combination of the AAPA and Mehrotra fails to do so, Applicant respectfully submits that claim 5 is allowable over the cited prior art.

Claim 8

Claim 8 recites in-part conducting a search of a SRAM and DRAM lookup table includes searching an SRAM portion for routing information, wherein if routing information is found in the SRAM portion, no search is performed in an DRAM portion, and wherein if no routing information is found in the SRAM portion, searching the DRAM portion of the SRAM and DRAM lookup table.

As discussed *supra*, the proposed combination of the AAPA and Mehrotra fails to arrive at the claimed invention, because Mehrotra does not teach the foregoing claimed limitations.

Thus, for analogous reasons with respect to claim 1, Applicant respectfully submits that claim 8 is allowable over the cited prior art.

Claim 12

Claim 12 recites in-part a routing table having a DRAM portion and an SRAM cache, wherein a first portion of a search of the routing table is conducted in the SRAM cache and a

second portion is conducted in the DRAM portion, and wherein the second portion of the search is conducted only if no routing information is found in the SRAM portion.

As discussed *supra*, the proposed combination of the AAPA and Mehrotra fails to arrive at the claimed invention, because Mehrotra does not determine searching the DRAM off-chip memory if such a need exists, or searching the DRAM off-chip memory only if routing information is not found in the SRAM on-chip memory.

Thus, as each and every limitation must be either disclosed or suggested by the cited prior art in order to establish a *prima facie* case of obviousness (see, **M.P.E.P. § 2143.03**), and the combination of the AAPA and Mehrotra fails to do so, Applicant respectfully submits that claim 12 is allowable over the cited prior art.

III. All Dependent Claims Are Allowable Because The Independent Claims From Which They Depend Are Allowable

Under Federal Circuit guidelines, a dependent claim is neither anticipated nor rendered obvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co., 819 F.2d at 1100, 1108 (Fed. Cir. 1987)*. Accordingly, as independent claims 1, 5, 8 and 12 are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also in condition for allowance.

With respect to claims 3, 6, 10 and 14, these claims are rejected under 35 U.S.C. § 103(a) as being unpatentable over the AAPA in view of Mohrota, and further in view of USP No. 6,154,746 to Berchtold. Applicant respectfully disagrees for the reasons set forth below.

Non-Analogous Art

Berchtold discloses a method for use in database management and database table. The method includes transforming multi-dimensional data points into 1-dimensional values, which are then stored in a 1-dimensional index structure. Specifically, Berchtold discloses using a Pyramid-Technique, which is based on a special partitioning strategy for optimizing high-dimensional data.

In the pending rejection, the Examiner applies the bisection or interval search algorithms cited in col. 15 of Berchtold to the SRAM/DRAM memory of the lookup table rendered by the combination of the AAPA and Mehrotra. However, the bisection or interval search algorithms of Berchtold are used in conjunction with a B+-tree used in a computer database system (e.g., index files are commonly configured in a B-Tree structure). Accordingly, Applicant respectfully submits that the bisection or interval search algorithms of Berchtold used in computer database applications and the physical memory structures of the AAPA and Mehrotra are directed to different aims and have different functions, and are thereby non-analogous.

Therefore, the proposed combination fails to establish *prima facie* obviousness of claims 3, 6, 10 and 14.

IV. Conclusion

By responding in the foregoing remarks only to particular positions taken by the Examiner, the Applicant does not acquiesce with other positions that have not been explicitly addressed. In addition, Applicant's arguments for the patentability of a claim should not be understood as implying that no other reasons for the patentability of that claim exist.

For all of the reasons set forth above, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicant's attorney at the telephone number shown below.

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Serial No. : 10/052,793
Filed : November 2, 2001
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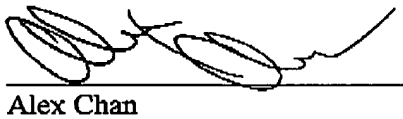
Attorney's Docket No.: 12754-169001 / 2001P16199US

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 06-1050 and please credit any excess fees to such deposit account.

Respectfully submitted,



Date: June 2, 2006

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